Aniotek Inc.
Softing Industrial Automation GmbH

UNIFIED FIELDBUS CONTROLLER
UFC100-L2

DATA SHEET

COPYRIGHT NOTICE

For further information contact:

Aniotek Inc.
10 April Drive
Dayton, NJ 08810
+1 732 274 2648
info@aniotek.com

Softing Industrial Automation GmbH
Richard-Reitzner-Allee 6
85540 Haar, Germany
Phone: +49 89 456 56 – 340
info.automation@softing.com

Revision History

Rev. no.	Reason for change
1.0	Released UFC100-L2, the second source from another foundry, technical changes are documented in 1.5 Changes between UFC100-L1 and UFC100-L2. The Version number read from register 0x00 has changed – see Table 2: Basic mode registers
1.1	Corrected the jitter specifications in Table 11: MAU Interface Timings.

TABLE OF CONTENTS

1 INTRODUCTION

The UFC100-L2 (Unified Fieldbus Controller) is a peripheral that that can be used in a Fieldbus Device or Host to provide a complete solution for implementing Fieldbus equipment. The UFC100-L2 includes all of time-critical functions in the hardware. It implements part of Physical and Data Link Layers for the Foundation Fieldbus H1 and Profibus-PA. This document shows the pin signals, electrical specifications and package dimensions.

1.1 Overview

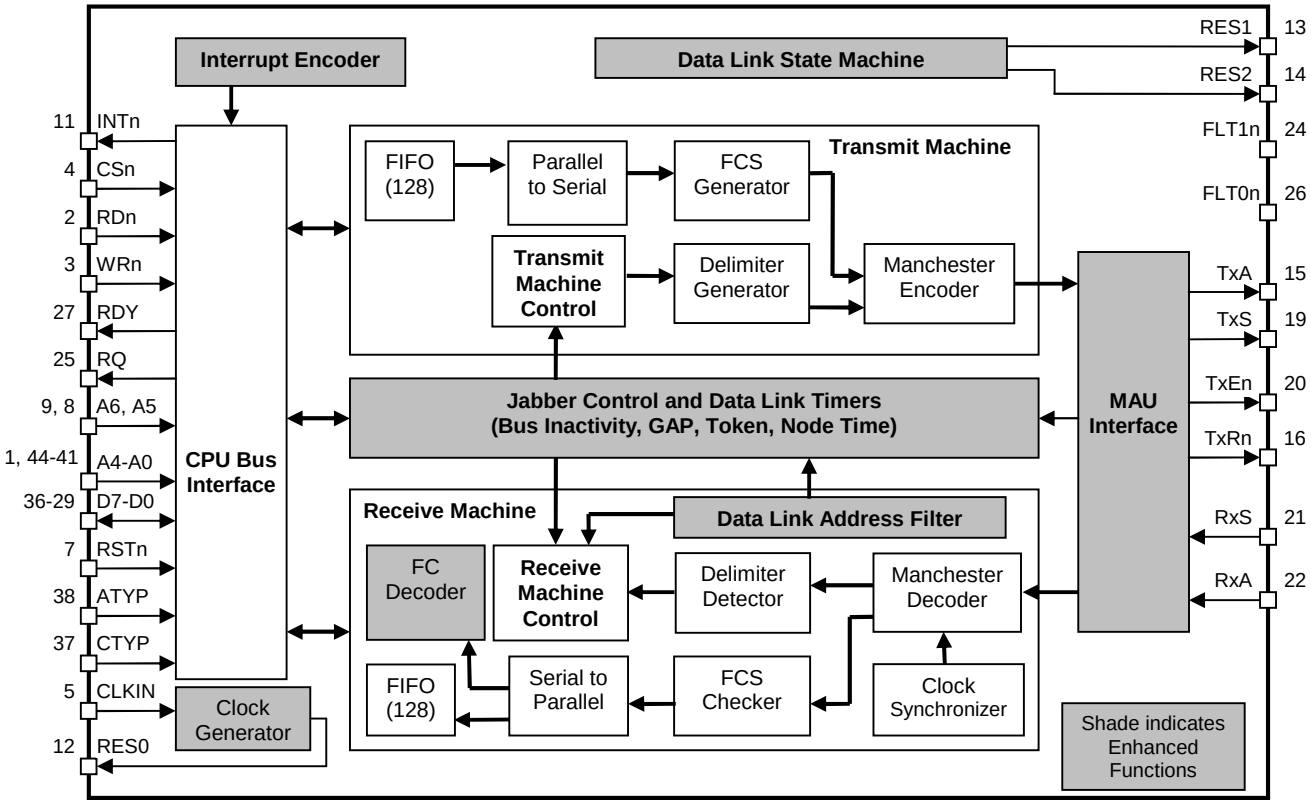

Figure 1: UFC100-L2 Block Diagram

1.2 Features

It is:

- Compliant to IEC 61158-2 Physical layer at 31.25 Kbit/s,
- Compliant to IEC 61158-4 Data Link layer,
- RoHS certified 44 pin LQFP package,
- Operating voltage 2.7 to 3.6 V,
- Low current consumption suitable for Field devices,
- Flexible 8-bit CPU bus interface suitable for all types of processors,
- 128 byte Transmit and Receive FIFO to reduce the number of the interrupts to the CPU.

1.3 Applications

The UFC100-L2 can be used for

- FF-H1 Fieldbus Device,
- PROFIBUS-PA Fieldbus Device,
- H1 Host Interface,
- HSE Linking Device.

1.4 Ordering Information

UFC100-L2 Unified Fieldbus Controller in LQFP package

IFL-KK-020911: delivered in trays

IFA-KK-020914: delivered as tape&reel

1.5 Changes between UFC100-L1 and UFC100-L2

The UFC100-L2 has function, package and pins same as UFC100-L1, except in L2 the following pins are not 5 V tolerant.

Pin	Signal
7	RESETn
21	RxS
22	RxA
26	FLT0n
37	CTYP
38	ATYP

The UFC100-L2 draws lower current for its operation – see 4.2.1 Current Consumption.

1.6 PIN Description

The following conventions are used.

Name If the name ends in ‘n’ then that signal is active low.

Type It specifies the type of input or output.

P	Power
ICH	Input – CMOS with hysteresis
O	Output – always active
BCH	Input / Output CMOS with hysteresis

Reset value For output signals, it specifies the value when external (hardware) reset is applied.

H	High
L	Low
TS	Tristate

Table 1: UFC100-L2 Pin out

Pin no.	Name	Type	Reset value	Description
1	A4	ICH		CPU Address bus
2	RDn/EDSn	ICH		Read Strobe (Intel mode), E or DSn (Freescale mode)
3	WRn/RWn	ICH		Write Strobe (Intel mode), RWn – Read or Write select (Freescale mode)
4	CSn	ICH		Chip Select – active state enables Read or Write access.
5	CLKIN	ICH		Clock input – the frequency has to be one of 1, 2, 4 or 8 Mhz.
6	Vss	P		Power negative side
7	RESETn	ICH		Reset – active (low).
8	A5	ICH		This pin can be connected to CPU address A5, or to Vdd or Vss.
9	A6	ICH		This pin can be connected to CPU address A6, or to Vdd or Vss.
10	MS2	ICH		Reserved for test use; connect it to Vss.
11	INTn	O	H	Interrupt request to the CPU
12	RES0	O	L	Reserved
13	RES1	O	L	Reserved
14	RES2	O	L	Reserved
15	TxA	O	L	It is used as TxA output, which is high while transmitter is active.
16	TxRn	O	H	Low pulse of 8 µs duration whenever TxS changes.
17	Vdd	P		Power plus side
18	Vss	P		Power negative side
19	TxS	O	L	Transmit signal to medium attachment unit
20	TxEn	O	H	Transmit control to medium attachment unit
21	RxS	ICH		Receive Signal from medium attachment unit
22	RxA	ICH		Receive activity (carrier detect) from medium attachment unit
23	TST0	ICH		Test input; connect to Vss in normal operation.
24	FLT1n	ICH		Not used – this pin can be connected either Vss or Vdd.
25	RQ	O	L	DMA request output, one pulse per byte to be transferred
26	FLT0n	ICH		Not used – this pin can be connected either Vss or Vdd.
27	RDY DACKn	O	H H	ATYP high: low value indicates that the data is ready or accepted. ATYP low: high value indicates that the data is ready or accepted.
28	Vss	P		Power negative side
29	D0	BCH	TS	CPU Data bus
30	D1	BCH	TS	CPU Data bus
31	D2	BCH	TS	CPU Data bus
32	D3	BCH	TS	CPU Data bus
33	D4	BCH	TS	CPU Data bus
34	D5	BCH	TS	CPU Data bus
35	D6	BCH	TS	CPU Data bus
36	D7	BCH	TS	CPU Data bus
37	CTYP	ICH		Type of CPU – Low: Intel, High: Freescale
38	ATYP	ICH		Type of bus access – Low: RDY output, High: DACKn output
39	Vdd	P		Power plus side
40	Vss	P		Power negative side
41	A0	ICH		CPU Address bus
42	A1	ICH		CPU Address bus
43	A2	ICH		CPU Address bus
44	A3	ICH		CPU Address bus

2 BASIC MODE

2.1 Operation

2.1.1 Transmit Machine

It has 128 byte Transmit FIFO. For most of the frame types, the CPU can write the entire frame to this memory. The automatic FCS can be disabled for test purpose. The Transmission starts only when the gap from the immediately prior reception or transmission is more than or equal to the programmed minimum Gap. Transmission starts by sending a programmed number of Preamble bytes followed by the Start Delimiter. The transmission ends by sending any remaining bytes of the frame, followed by two FCS bytes, followed by End Delimiter. DMA can be used to transfer bytes to be transmitted from the memory to the FIFO.

2.1.2 Receive Machine

The received frame is stored in the 128 byte Receive FIFO. The signal polarity of the received signal is automatically corrected. For most frames, an interrupt is generated only after the entire frame has been stored in this memory. The CPU can cancel the current reception. The current reception is also cancelled if any error is detected, but the Receive FIFO is not cleared. The receiver does not write any more bytes to this FIFO. The error flag is set when the error is detected, but further errors are not registered. DMA can be used to transfer received bytes from the FIFO to the memory.

2.1.3 Data Link Timers

The Node Time counter keeps the value of Node time with a resolution of 1/4 ms or 1/32 ms depending upon another setting.

Watch-time counter is used to monitor Maximum-Response-Delay, Immediate-Response-Recovery-Delay and Token-Recovery-Delay. There is a filter on bus activity, so that noise does not reset this counter.

Gap counter is used to provide the minimum gap between two frames – it runs whenever there is no receive or transmit activity.

Jabber Counter is used to check the length of transmit frame or receive frame – it runs whenever there is transmit activity and jabber is enabled or there is receive activity and jabber is enabled.

Token counter is used as Remaining Token Duration timer. It is always loaded from the PT frame. It can be reloaded by the CPU any time. It counts down whenever it is non-zero.

2.1.4 MAU Interface

It converts the internal transmit signals to TxE and TxS. The Transmit driver can be setup for Transmit Enable or ADD mode. The input RxA and RxS signals are converted to internal receive signals. The loopback modes can be setup for testing. Physical layer parameters such as Preamble extension and minimum Gap can be setup.

2.1.5 CPU Bus Interface

The UFC100-L2 can be connected to any synchronous or asynchronous bus. The type of CPU can be Intel or Freescale. The selection is done by two input pins. The data interface is 8-bit wide; the address bus is 5-bit wide.

2.2 Basic mode registers

Table 2: Basic mode registers

Address HEX	Name	Access Read/ Write	Reset value	Description
00	Reset, Version	R/W	0x30	Software reset**, UFC100-L2 Version**
01	Mode	R/W	0x00	Selection of operating modes
02	Control	R/W	0x00	Control functions
03	Status	R/-	0x82	Shows status
04	Interrupt status	R/-	0x00	Shows reason of interrupts
05	Error status	R/-	0x00	Shows reason of communication errors
06	Interrupt mask	R/W	0xFE	Mask for interrupts
07	Error mask	R/W	0xFB	Mast for error interrupts
08	Tx length (LOW)	R/W	0x00	Length of transmitted frame (Lower byte)
09	Tx length (HIGH)	R/W	0x00	Length of transmitted frame (Higher 2 bits)
0A	Reserved	-/-	--(1)	Not used
0B	FIFO control	R/W	0x00	Control register of FIFO
0C	FIFO status	R/-	0x11	Shows status of FIFO
0D	DATA	R/W	0x00	Transmit/Receive data to/from FIFO
0E	Reserved	-/-	--(1)	Not used
0F	Reserved	-/-	--(1)	Not used
10	Clock mode	R/W	0x00	DL mode, Timer enables
11	Timer status	R	0x00	Node-timer status
12	Node time (LOW)	R/W	0x00	Timer to hold DL NODE time (Lower byte)
13	Node time (HIGH)	R/W	0x00	Timer to hold DL NODE time (Higher byte)
14	Gap time	-/W	0xFF	Value to generate minimum inter-PDU delay
15	Reserved	-/-	--(3)	Not used
16	Watch time (LOW)	-/W	0xFF	Value to detect no-activity of bus (Lower byte)
17	Watch time (HIGH)	-/W	0xFF	Value to detect no-activity of bus (Higher byte)
18	Token counter (LOW)	R/W	0x00	Remaining token holding time (Lower byte)
19	Token counter (HIGH)	R/W	0x00	Remaining token holding time (Higher byte)
1A	Timer control	R/W	0x00	Control DL timers
1B	Reserved	-/-	--(1)	Not used
1C	Reserved	-/-	--(1)	Not used
1D	Reserved	-/-	--(1)	Not used
1E	Reserved	-/-	--(1)	Not used
1F	Reserved	-/-	--(1)	Not used
(1): Unused registers read as 0x00.				

2.3 Performance Improvement

Even with existing software, UFC100-L2 reduces the number of the interrupts to the CPU and thus provides performance improvement. There is filter on bus activity to make it less sensitive to noise.

3 EXTERNAL INTERFACES

The UFC100-L2 operates at 2.7 – 3.6 volts. All inputs and outputs require that the voltage does not exceed power supply voltage.

The external interface signals are divided into following groups:

Clock input,
CPU Bus,
MAU, and
Others.

3.1 Clock Input

The UFC100-L2 can work at clock rate of 1, 2, 4 or 8 Mhz.

3.2 CPU Bus Interface

The UFC100-L2 has 8-bit wide data bus and 5 bit address bus interface. It can be connected to most of the CPU types without any 'glue' logic. It always indicates the completion of the access on 'RDY / DACKn' output pin.

1. If the CPU uses multiplexed address and data lines, then the external circuit has to use a latch to store the address.
2. It always indicates the completion of the access on 'RDY / DACKn' output pin. A CPU does not have to use 'RDY / DACKn' signal, if it can be programmed with wait states. The worst case cycle time is four (4) periods of CLKIN input.
3. If the CPU uses a bus that runs at a higher clock rate than CLKIN input of UFC100-L2 and if the CPU cannot use 'RDY / DACKn' signal and if the CPU cannot insert enough wait states, then it has to use software to poll a status bit (ARDY) inside UFC100-L2. This bit indicates that it is ready for next cycle.
4. The inputs A6 and A5 can be connected to '0'. These addresses are not used.
5. If the microcontroller does not support DMA, then do not connect RQ output.
6. If the microcontroller supports DMA or DMA controller is available, then use RQ. This output has one pulse for each byte to be transferred. The active polarity of this pulse is high.
7. The reset input can be connected to either an output port of the microcontroller or its reset input.

Table 3: CPU Bus type connections

CTYP (pin 37)	ATYP (pin 38)	CPY type	Description
0	0	Intel	Pin 2 is RDn – Read Strobe, active low. Pin 3 is WRn – Write Strobe, active low. Pin 27 is RDY – a high indicates the cycle can be completed.
0	1	Intel	Pin 2 is RDn – Read Strobe, active low. Pin 3 is WRn – Write Strobe, active low. Pin 27 is DACKn – a low indicates the cycle can be completed.
1	0	Freescale	Pin 2 is E – a high indicates start of the active part of the cycle. Pin 3 is RWn – a high indicates Read cycle. Pin 27 is RDY – a high indicates the cycle can be completed.
1	1	Freescale	Pin 2 is DSn – a low indicates start of the active part of the cycle. Pin 3 is RWn – a high indicates Read cycle. Pin 27 is DACKn – a low indicates the cycle can be completed.

3.2.1 Renesas CPU with RDY

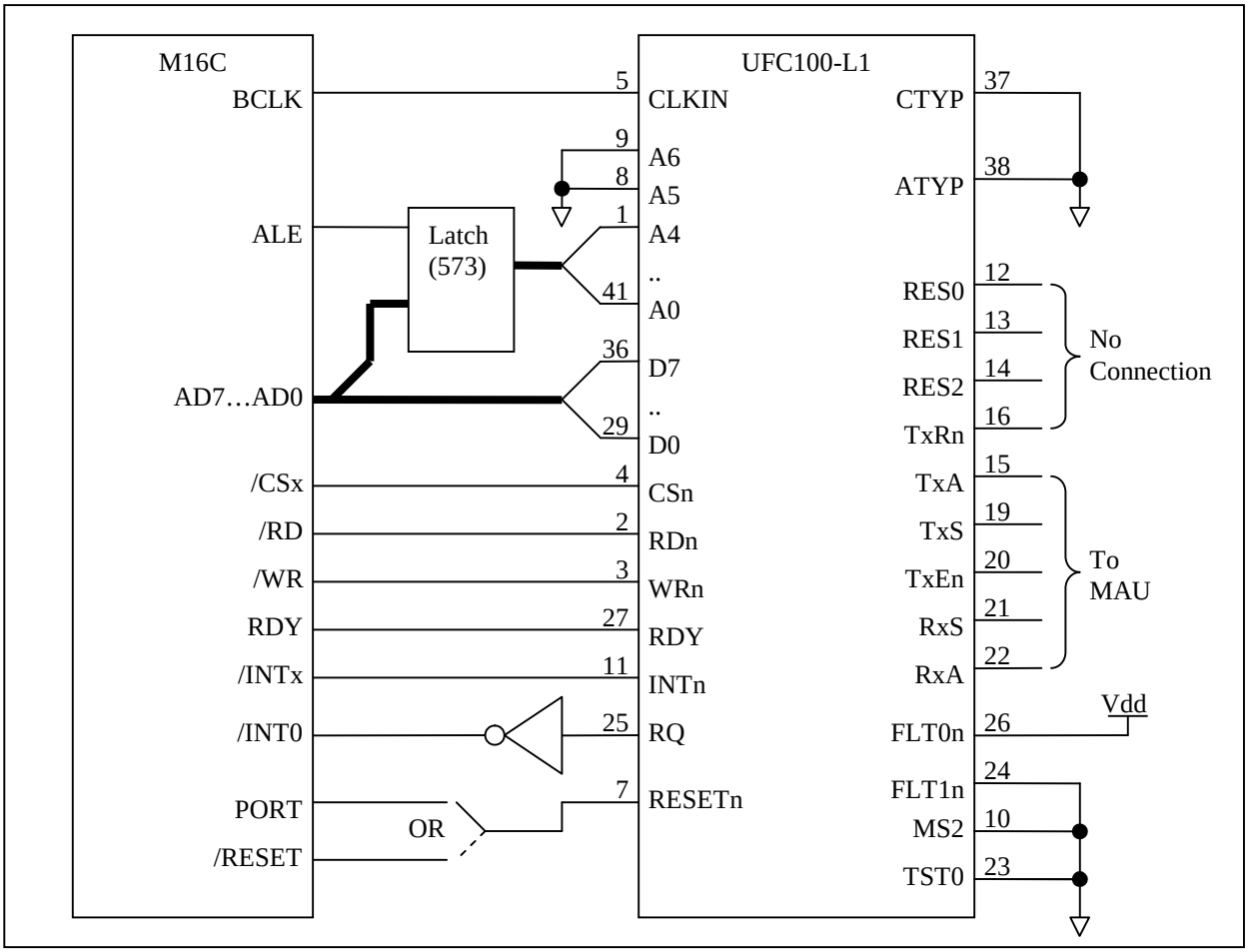

Figure 2: Interface to Renesas M16 using Multiplexed Bus

This type of interface requires separate Read and Write control signals. The UFC100-L2 provides RDY signal, which is normally high. It may become low at the start of the Read or Write cycle to indicate that the CPU has to wait. It becomes high when the CPU can complete the cycle. The Figure 2 shows interface to Renesas microcontroller. This example is meant for existing designs.

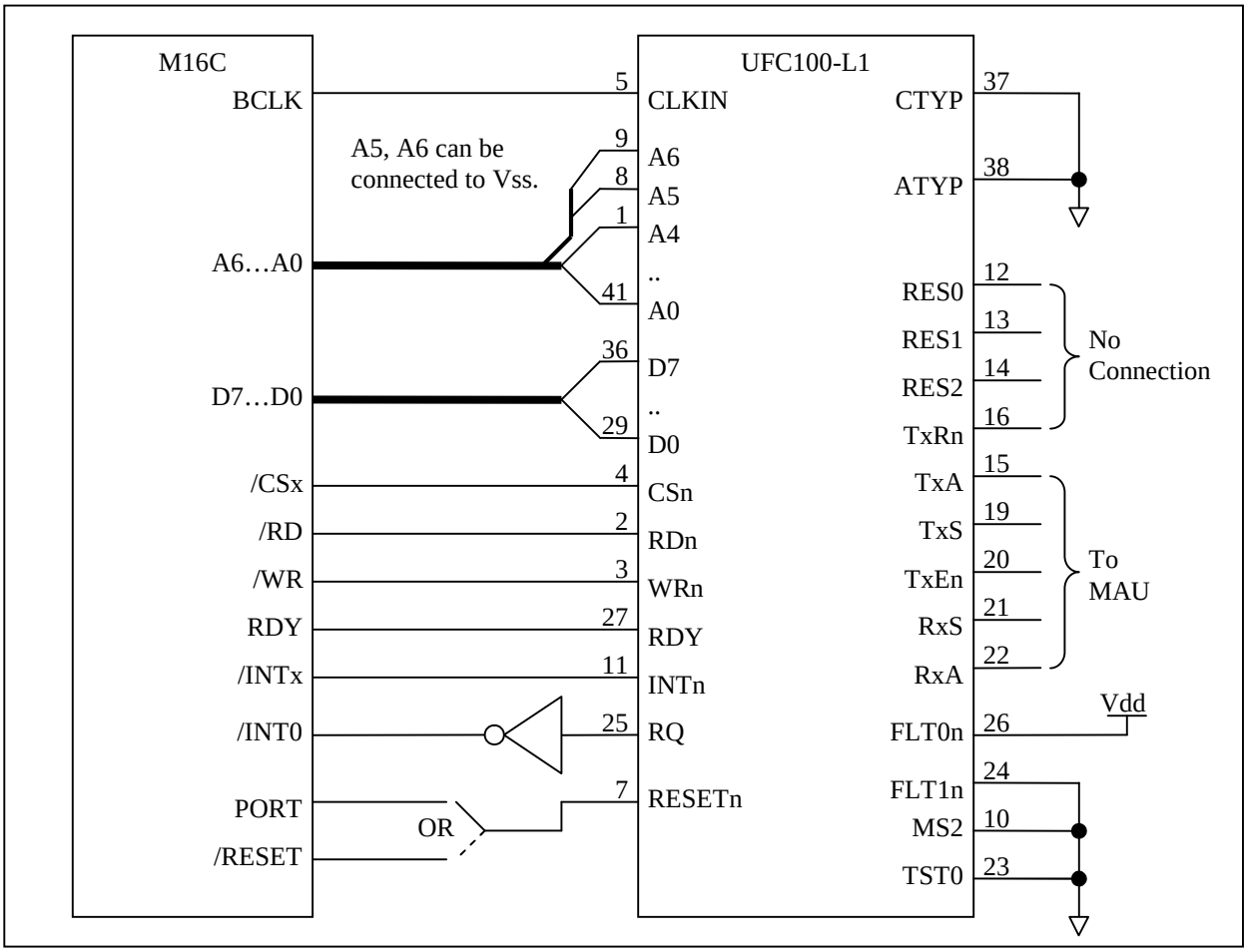

Figure 3: Interface to Renesas M16 using Non-multiplexed Bus

The newer design can use the non-multiplexed bus as shown in the Figure 3. The /INT0 input is used for DMA request.

3.2.2 Intel X86 Type CPU with /READY

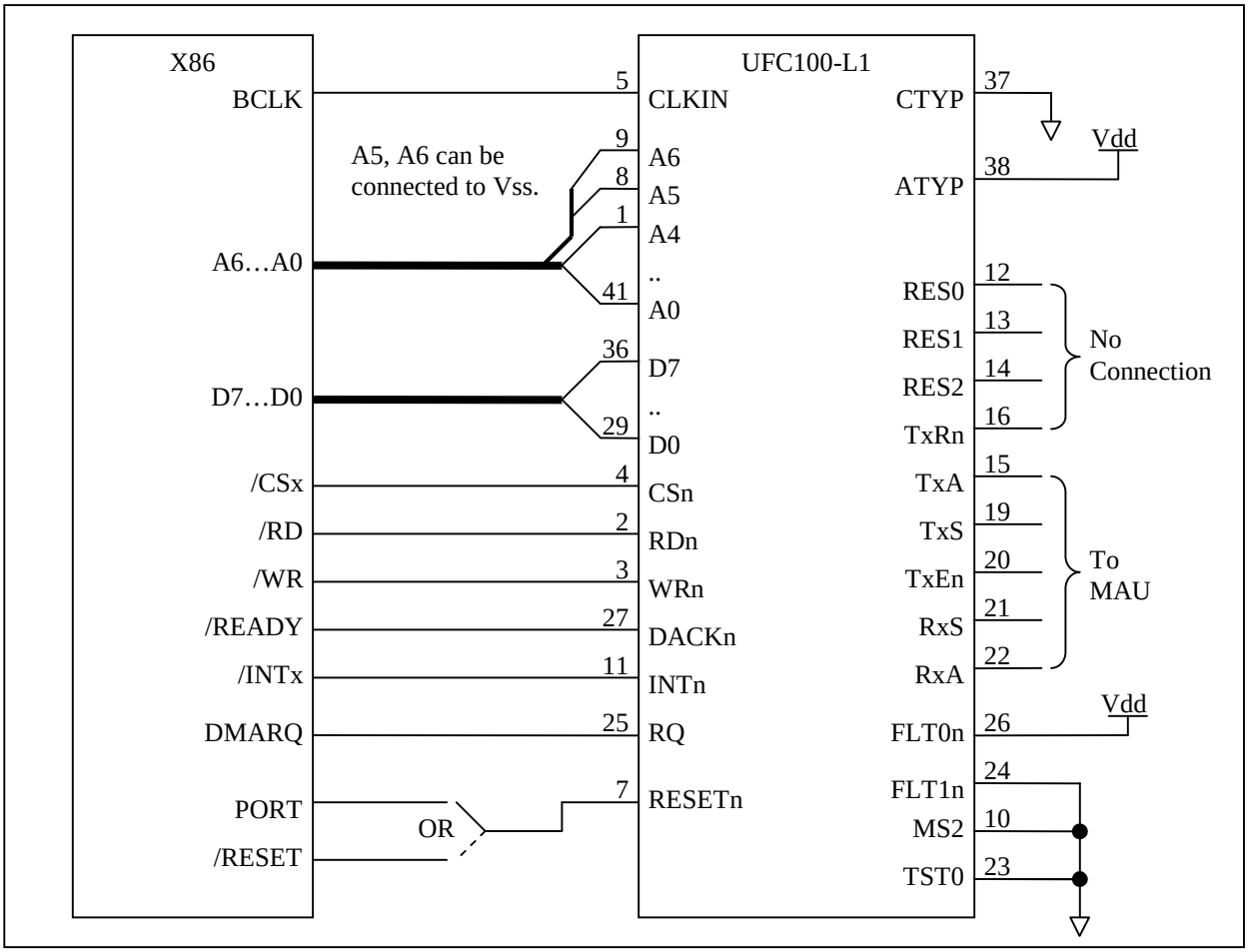

Figure 4: Interface to Intel Type CPU with /READY

This type of interface requires separate Read and Write control signals. It provides a DACKn signal, which is normally high. It becomes low towards the end of a Read or Write cycle to indicate to the CPU that it can complete the cycle. It becomes high when the CPU completes the cycle. The Figure 4 shows interface to such CPU. This example is meant for new designs, because the polarity of the output at pin 27 is reversed.

3.2.3 Freescale Type CPU with /DTACK, Existing Design

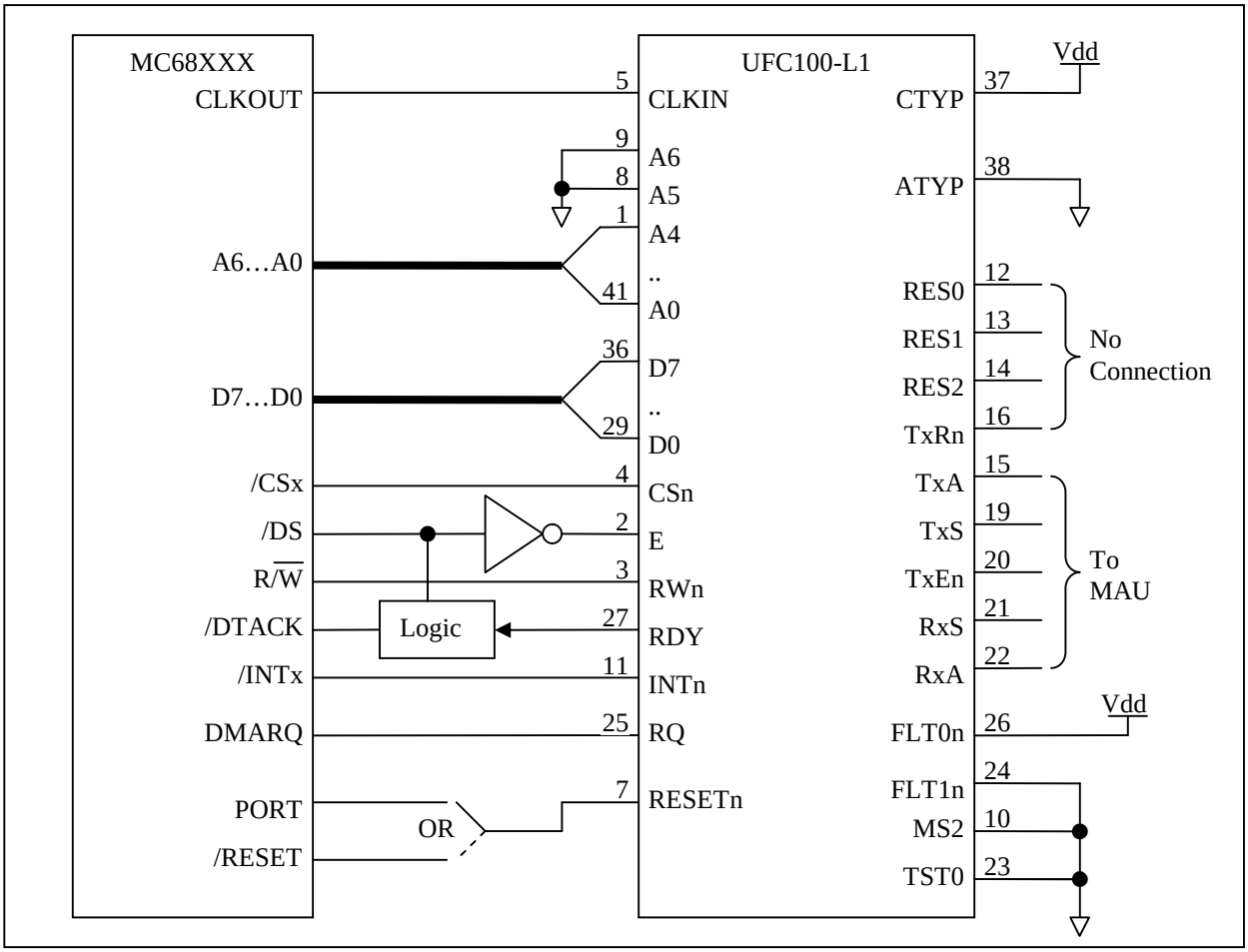

Figure 5: Interface to Freescale MC683XX, MC68C16 – existing designs

This type of interface requires a common data strobe and another signal for Read, Write control. It provides a RDY signal, which is normally high. It may become low at the start of the Read or Write cycle to indicate that the CPU has to wait. It becomes high when the CPU can complete the cycle. The RDY output requires some amount of logic to convert it to /DTACK signal. The Figure 5 is meant for existing designs, because it requires inverter and logic for two control signals.

3.2.4 Freescale Type CPU with /DTACK, New Design

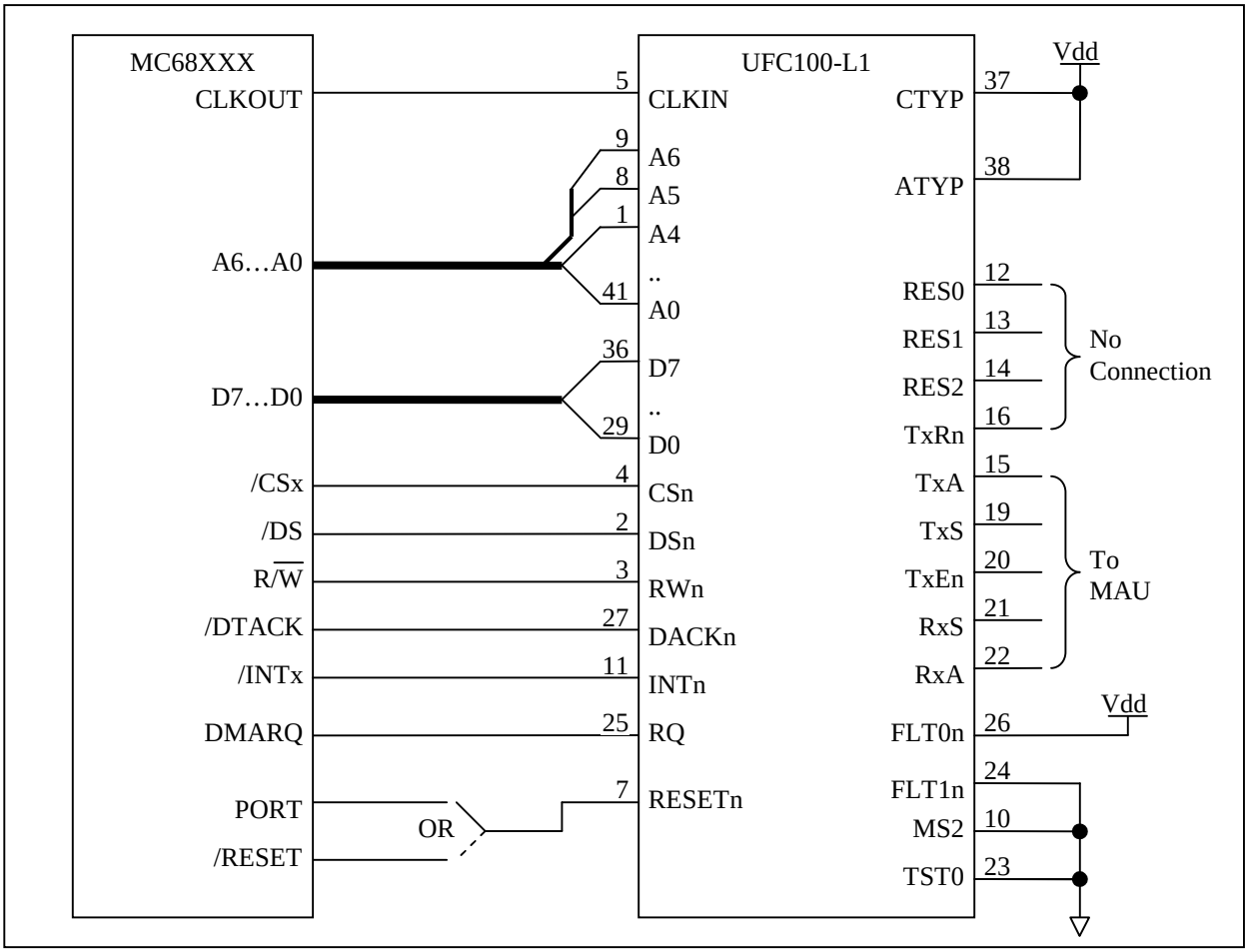

Figure 6: Interface to Freescale MC683XX, MC68C16 – new designs

This type of interface requires a common data strobe and another signal for Read, Write control. The UFC100-L2 provides a DACKn signal, which is normally high. It becomes low towards the end of a Read or Write cycle to indicate to the CPU that it can complete the cycle. It becomes high when the CPU completes the cycle.

3.2.5 Power PC

The PowerPC has a bus interface which is similar to Intel type CPU. It has /OE and /WE signals which can be connected to RDn and WRn inputs of the UFC100-L2. It can be programmed for various number of wait states.

3.3 MAU Interface

This interface consists of four signals – TxEn, TxS, TxRn and TxA for Transmitter and two signals – RxA and RxS for Receiver. These MAU signals are specified in 3.3.1 and 3.3.2.

3.3.1 Transmitter Interface

The two signals – TxEn and TxS can be setup for Enable or ADD mode as shown in the Table 4.

Table 4: MAU Transmit Modes

Transmit Mode	TxEn	TxS	Operation
Enable Low	1	0	Transmitter Inactive
	1	1	Transmitter Inactive
	0	0	Transmit '0'
	0	1	Transmit '1'
ADD	1	0	Transmitter Inactive
	0	1	Transmitter Inactive
	0	0	Transmit '0'
	1	1	Transmit '1'

The TxA signal is always high during active transmission for all transmit modes. It can be used to enable the transmit buffer in the MAU that drives voltage or to change the bias current in the MAU that modulates the current. It can also be used to drive an LED to show active transmission. This signal stays high for 4 µs after the end of the transmission, so that the MAU can drive the transmission line to inactive state. TxRn signal is high during inactive transmission. It changes from high to low every time TxS has a transition. It remains low for 8 µs for all transitions, except at the start and the end of the transmission. The start and end low duration is 4 µs.

3.3.2 Receiver Interface

The two signals – RxA and RxS are shown in the Table 5.

Table 5: MAU Receive Mode

Receive Mode	RxA	RxS	Indication
Level high	0	1	Receive Inactive
	0	0	Receive Inactive
	1	0	Receive '0'
	1	1	Receive '1'

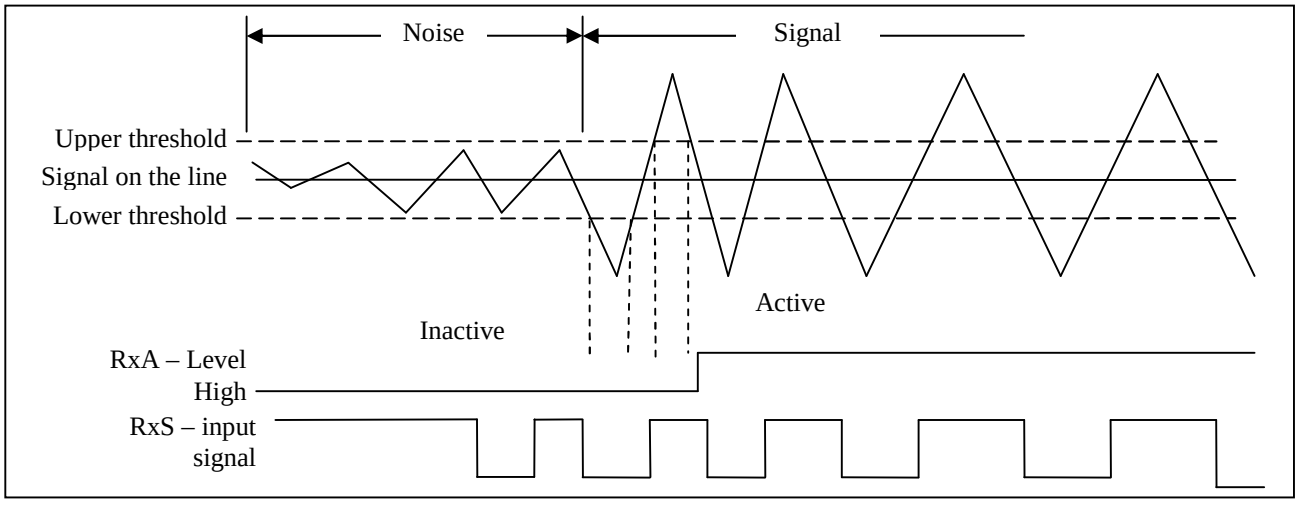

Figure 7: Carrier Detect (RxA) and Signal (RxS) inputs

RxS signal should be generated by comparing the analog received signal with zero and thus it can become active due to noise as shown in the Figure 7. The external MAU should generate active RxA signal only after detecting sufficient activity beyond the noise threshold and for sufficient time, so that noise above threshold can also be filtered. After the noise filter, RxA signal should be continuous level as long as the signal level and duration is considered to be sufficient to infer a valid signal. Receiver does not filter RxA signal. The RxS is considered valid only when RxA is active.

3.4 Other Interfaces

3.4.1 Reset and Interrupt Signals

Table 6: Reset and Interrupt Signals

Signal	Description
RESETn	A low value at this input resets all of the UFC100-L2.
INTn	This output becomes active when it needs to interrupt the CPU. The active polarity is low. This signal stays active as long as any one of the interrupt sources in the UFC100-L2 is active.

The reset signal should be applied as soon as possible after the power is applied. The clock can become active after reset signal is applied. But, the reset should not be removed until after the clock input CLKIN has become active. The VDD power must be at least at the required minimum operating value when reset is removed.

4 ELECTRICAL AND TEMPERATURE SPECIFICATIONS

4.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	Supply Voltage	– 0.3	4.0	V
VI	DC Input Voltage	– 0.3	V_{DD} + 0.3	V
VO	DC Output Voltage	– 0.3	V_{DD} + 0.3	V
T_J	Junction Temperature	– 40	125	^{0} C

4.2 Operating Conditions

Symbol	Parameter and condition	Min	Typical	Max	Units	Note
V_{DD}	Supply voltage	2.7		3.6	V	
	DC input voltage	0		V_{DD}	V	
VIL	Input low voltage – ICH type	0		0.3*V_{DD}	V	
VIH	Input high voltage – ICH type	0.7*V_{DD}		V_{DD}	V	
VH	Input hysteresis		0.4		V	
IL	Input leakage current			5	µA	
VOL	Output low voltage @ IOL = 0.1 mA			0.2	V	
VOL	Output low Voltage RES0, RES1, RES2 @ IOL = 8 mA D7 – D0, RDY @ IOL = 4 mA All other outputs @ IOL = 2 mA			0.5	V	
VOH	Output high voltage @ ION = – 0.1 mA	V_{DD} – 0.2				
VOH	Output high Voltage RES0, RES1, RES2 @ IOL = 8 mA D7 – D0, RDY @ IOL = 4 mA All other outputs @ IOL = 2 mA	V_{DD} – 0.8			V	
VO	Voltage applied to tristate output	0		V_{DD}	V	
	Tristate output leakage current			5	µA	
Topr	Operating Temperature	– 40		85	^{0} C	
I_{DD}	Operating Current consumption @ 3 V @ CLKIN frequency = 2 MHz @ CLKIN frequency = 4 MHz Operating Current consumption @ 3.3 V @ CLKIN frequency = 8 MHz All inputs connected to CMOS outputs, All outputs driving CMOS inputs.		 0.25 0.30 0.45		mA	

4.2.1 Current Consumption

The typical operating current for most applications is less than 1 mA. The current consumption is shown in the Figure 8 and Figure 9 below. It was measured while the device was continuously transmitting and receiving in full duplex using DMA, with continuous Read and Write access to the device.

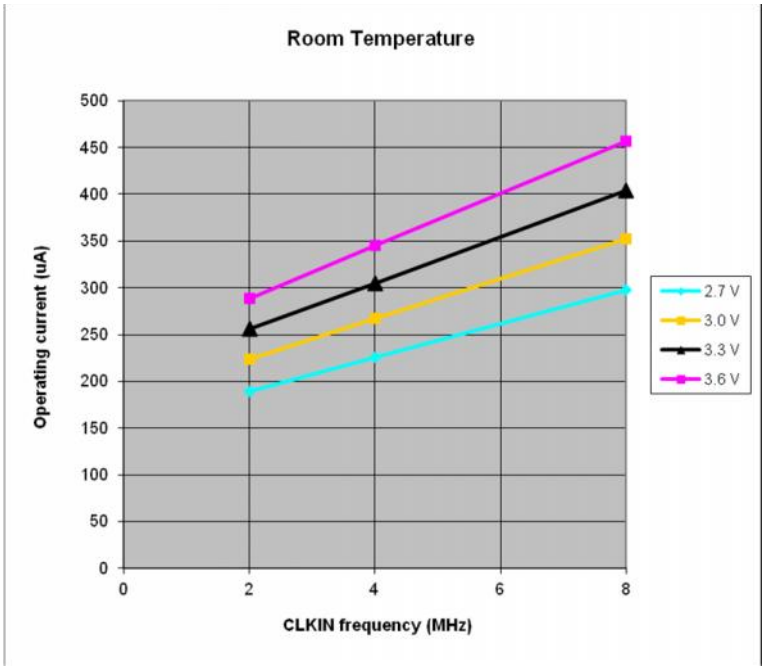

Figure 8: Typical operating current vs. frequency and voltage

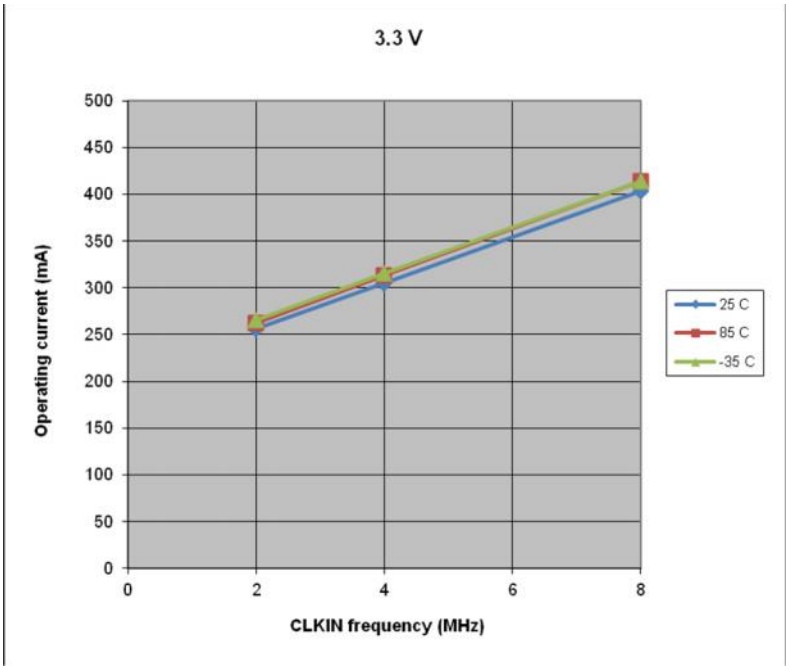

Figure 9: Typical operating current vs. frequency and temperature

The operating current at high temperature is slightly higher than current at room temperature. The operating current at low temperature is about the same as the current at room temperature.

4.3 Clock Input Timings

The timings are shown in the Table 7 and the Figure 10.

Table 7: Clock Timings

Name	Description	Min	Max
T_{CLK}	Clock input period @ V_{DD} = 2.7 to 3.6 V	125 ns	1000 ns
t_{CPWH}	Clock input pulse width high	10 ns	
t_{CPWL}	Clock input pulse width low	10 ns	

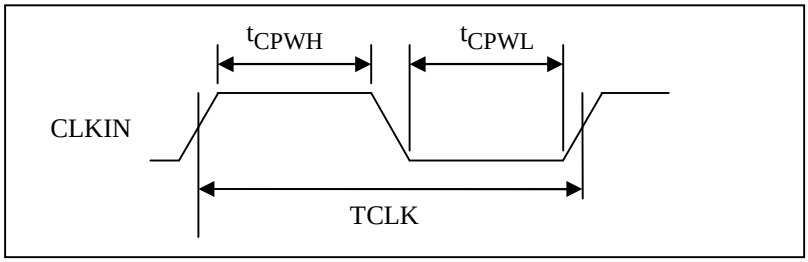

Figure 10: Clock Timings

4.4 CPU Bus Access Timings

The timing diagrams are shown for Read and Write access for all types of CPU. The CPU interface is asynchronous to CLKIN. However, internally the bus access is synchronized to CLKIN, for all Write accesses and for those Read accesses (FIFO, interrupt status, error status) that cause a Write. The successive accesses that cause Write have to be at least 4 clocks apart. This delay is indicated by the delay in RDY (DACKn) output. If the CPU can use RDY (DACKn) signal then it can issue successive access without delay. If the CPU cannot use RDY (DACKn) signal and if the successive bus access cannot be delayed then the CPU has to check completion of the prior access by reading a status register.

If Freescale type CPU with ‘E’ signal is connected, then replace ‘DSn’ signal in the timing diagrams by ‘E’ signal with inverted polarity.

The timings are shown in Figure 11, Figure 12, Table 8, Figure 13 Figure 14 and Table 9. The timing values for output signals are specified for a 50 pf load. All times are in ns unless specified otherwise.

4.4.1 Intel Type CPU

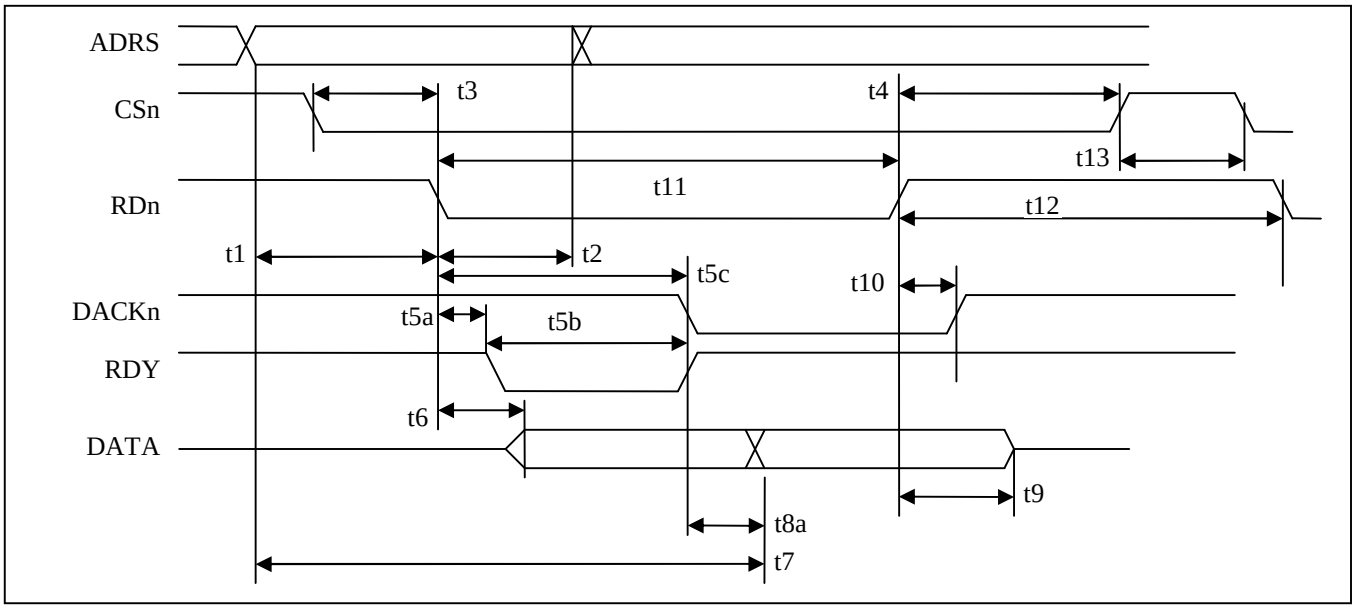

Figure 11: Intel Bus Read Cycle Timing Diagram

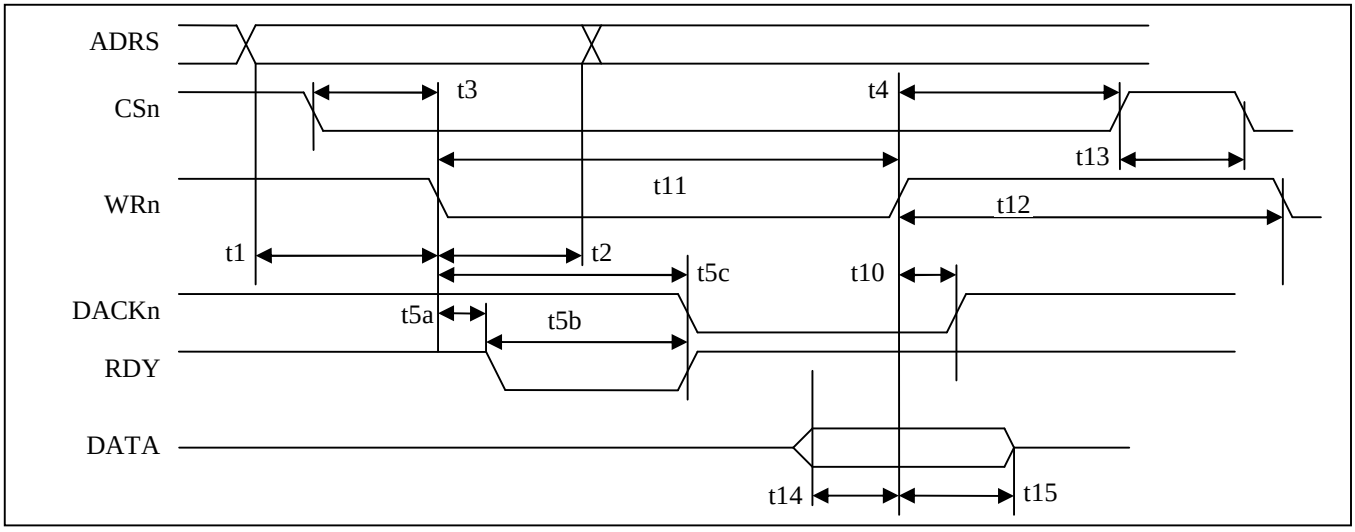

Figure 12: Intel Bus Write Cycle Timing Diagram

Table 8: Bus Timings for Intel type CPU

Num	Description	Min	Max	Notes
t1	Valid Address to RDn, WRn assertion (setup time)	10		
t2	RDn, WRn assertion to invalid Address (hold time)	10		
t3	CSn assertion to RDn, WRn assertion setup time	0		
t4	RDn, WRn negation to CSn negation (hold time)	0		
t5a	RDn, WRn assertion to RDY negation delay		20	3
t5b	RDY negation duration	0	4*TCLK 3*TCLK	1 2
t5c	RDn, WRn assertion to DACKn assertion delay	5	4*TCLK 3*TCLK	1 2
t5d	End of previous cycle to DACKn (RDY) assertion delay		4*TCLK + 30 3*TCLK + 30	3 2
t6	RDn assertion to active Data output delay		20	
t7	Valid address to valid data output access delay		30	
t8a	RDY (DACKn) to valid Data delay		20	3
t8b	Positive edge of CLKIN to valid Data delay		30	3
t9	RDn negation to tristate Data, invalid Data delay	3	15	
t10	RDn, WRn negation to DACKn negation delay	0	15	
t11	RDn, WRn assertion duration	10		
t12	RDn, WRn inactive time	10		
t13	CSn inactive time	10		
t14	Valid Data to WRn negation (setup time)		5	
t15	WRn negation to invalid Data (hold time)	5		

Notes:

1. This delay depends upon the immediately prior cycle. If there is sufficient gap between the two successive cycles, then RDY is not negated; DACKn assertion delay is 20 ns. The Write cycles and some of the Read cycles require that the end of the following cycle be spaced by 4*TCLK.
2. DACKn (RDY) can be asserted one clock earlier, if configured to do so by software. It requires that the delay from DACKn (RDY) assertion to RDn, WRn negation be at least one clock.
3. These delays apply only if RDY is negated. Otherwise, t7 applies. Use t8a only if the CPU cannot use CLKIN to synchronize the Read data input.

4.4.2 Freescale Type CPU

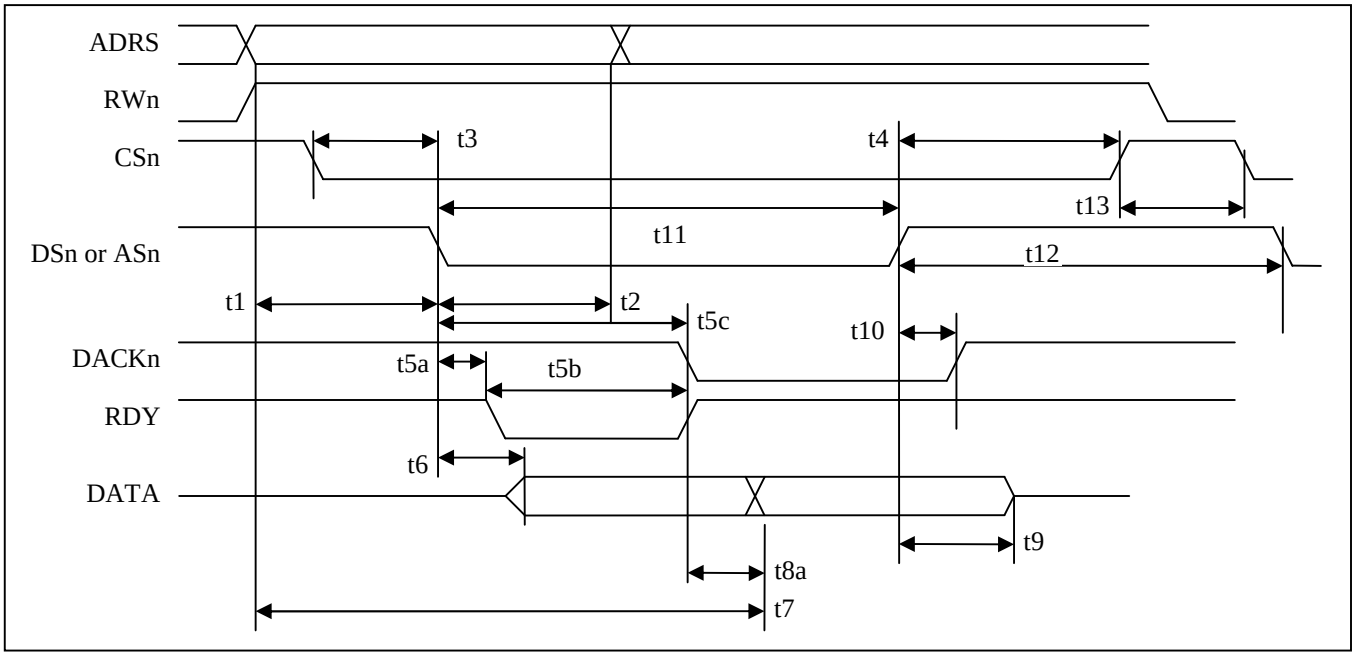

Figure 13: Freescale Bus Read Cycle Timing Diagram

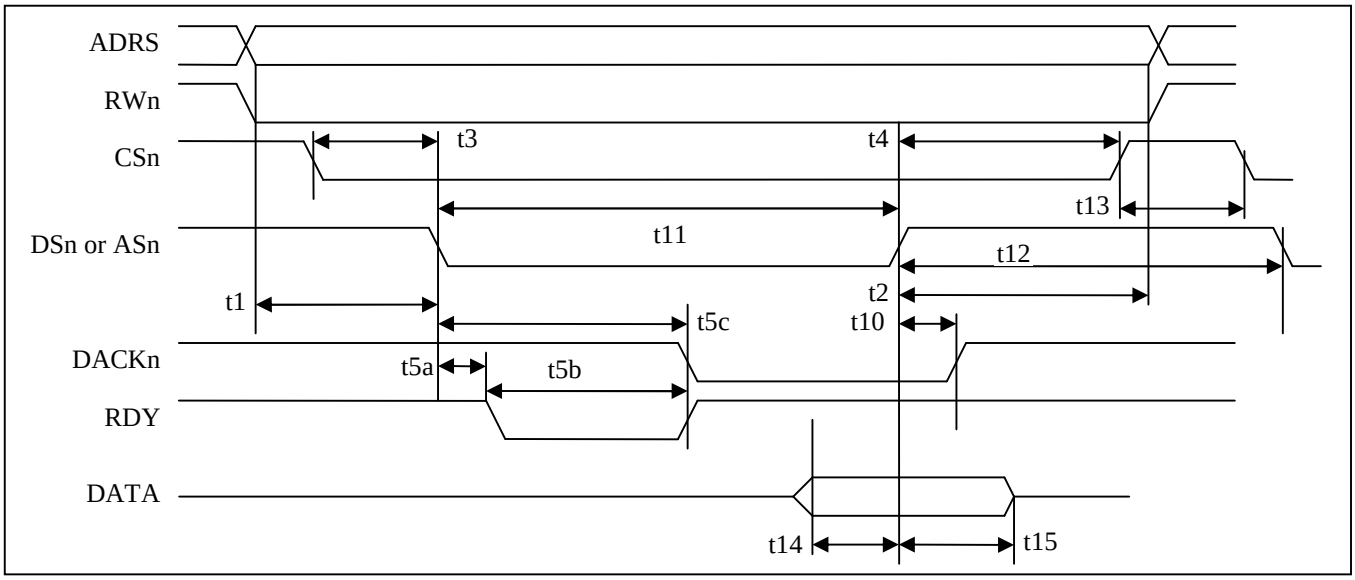

Figure 14: Freescale Bus Write Cycle Timing Diagram

Table 9: Bus Timings for Freescale type CPU

Num	Description	Min	Max	Notes
t1	Valid Address to DSn assertion (setup time)	10		
t2	DSn assertion to invalid Address (hold time)	10		
t3	CSn assertion to DSn assertion setup time	0		
t4	DSn negation to CSn negation (hold time)	0		
t5a	DSn assertion to RDY negation delay		20	3
t5b	RDY negation duration	0	4*TCLK 3*TCLK	1 2
t5c	DSn assertion to DACKn assertion delay	5	4*TCLK 3*TCLK	1 2
t5d	End of previous cycle to DACKn (RDY) assertion delay		4*TCLK + 30 3*TCLK + 30	3 2
t6	DSn assertion to active Data output delay		20	
t7	Valid address to valid data output access delay		30	
t8a	RDY (DACKn) to valid Data delay		20	3
t8b	Positive edge of CLKIN to valid Data delay		30	3
t9	DSn negation to tristate Data, invalid Data delay	3	15	
t10	DSn negation to DACKn (RDY) negation delay	0	15	
t11	DSn assertion duration	10		
t12	DSn inactive time	10		
t13	CSn inactive time	10		
t14	Valid Data to WRn negation (setup time)		5	
t15	WRn negation to invalid Data (hold time)	5		

Notes:

1. This delay depends upon the immediately prior cycle. If there is sufficient gap between the two successive cycles, then RDY is not negated; DACKn assertion delay is 20 ns. The Write cycles and some of the Read cycles require that the end of the following cycle be spaced by 4*TCLK.
2. DACKn (RDY) can be asserted one clock earlier, if configured to do so by software. It requires that the delay from DACKn (RDY) assertion to RDn, WRn negation be at least one clock.
3. These delays apply only if RDY is negated. Otherwise, t7 applies. Use t8a only if the CPU cannot use CLKIN to synchronize the Read data input.

4.4.3 DMA Request Timings

Table 10: DMA Request Timings

Num	Description	Min	Max
t_{RQD}	DMA transfer to inactive RQ delay	$2*T_{CLK}$	$4*T_{CLK}$
t_{RQP}	Pause between two successive RQ pulses	$4*T_{CLK}$	

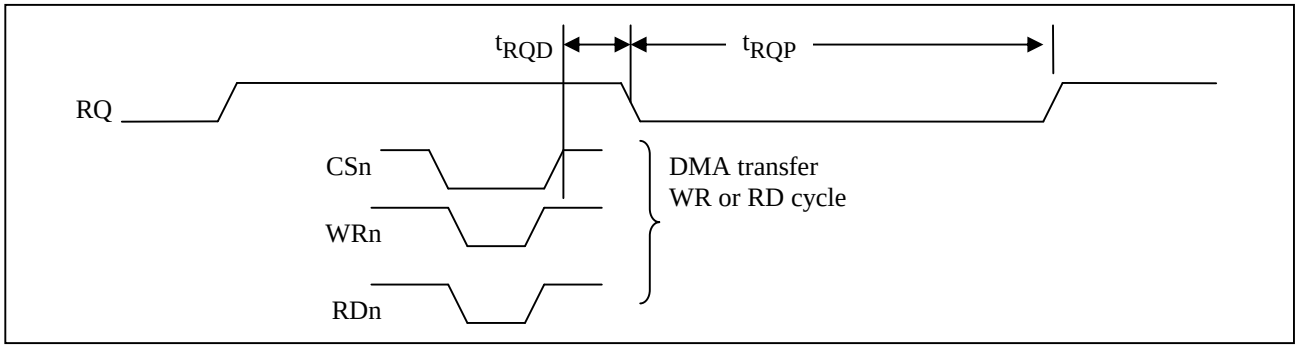

Figure 15: DMA Request Timings

4.5 MAU Interface Timings

The timings are shown in the Table 11 and the Figure 16 – Figure 18. The timings for output signals are specified for a 50 pf load.

4.5.1 MAU Interface Timings

Table 11: MAU Interface Timings

Num	Description	Min	Nom	Max	Notes
t_{TTR}	Transmit signal output transition time			20 ns	
t_{TSKW}	Skew between transitions in TxEn and TxS outputs			10 ns	
t_{TBIT}	Transmit bit average period		32 µs		1
t_{TXAD}	End of transmission of End Delimiter to TxEn, TxA delay		4 µs		1
t_{RBIT}	Receive signal input average period	30 µs		34 µs	
t_{RTR}	Receive signal input transition time			200 ns	
t_{RJTR}	Receive signal zero crossing jitter			± 3.75 µs	2
t_{LOCK}	Receive lock time			110 µs	3
t_{RxAH}	Receive activity signal hold time	0			

Notes:

1. This time depends upon the correct setting of internal clock. The average bit period has the same tolerance as the clock input tolerance. The bit to bit period jitter will be a small fraction (< 1/32) of the clock input period jitter.
2. This is at the RXS input to the UFC100 and after the first 6 bits of the PE (Preamble). The pulse width can vary by twice this jitter value.The theoretical max is 4 µs. The Recive filter between the Bus and the RXS can add 1.8 to 2.0 µs jitter. This filter adds only 0.1 µs jitter to the PE after it's first bit. A test of the 3000 meter Bus using RLC simulator shows that the Bus also adds only 0.1 µs jitter to the PE.
3. The Clock Synchronizer locks to the clock in RxS in maximum of four mid-bit transitions. Therefore, RxA signal has to be active at least 3.5 bit time before the end of Preamble.

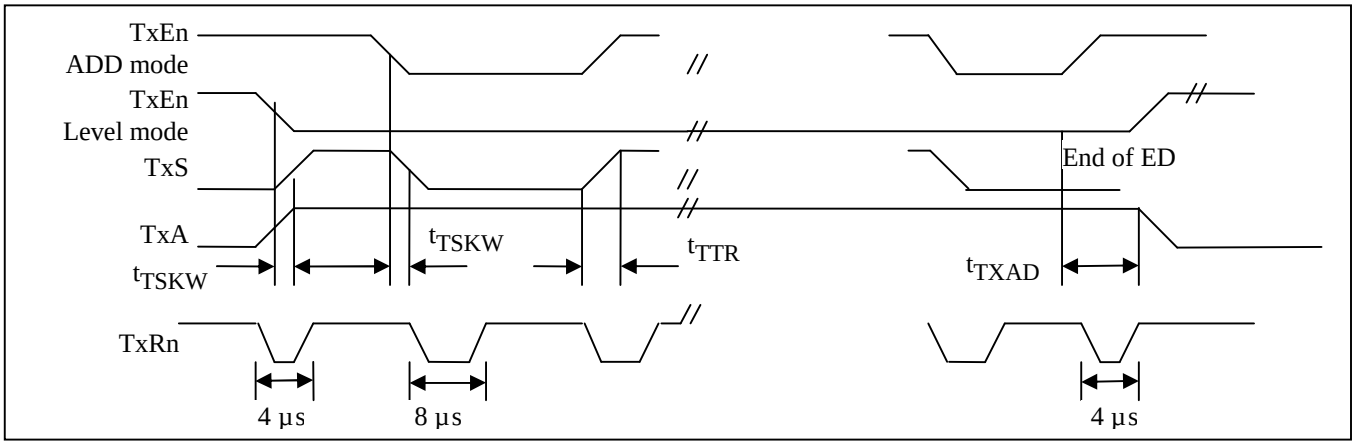

Figure 16: MAU Interface Transmit Signal Timings

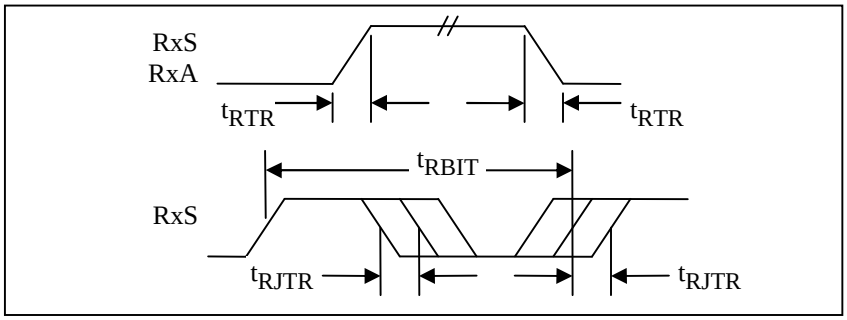

Figure 17: MAU Interface Receive Signal Timings

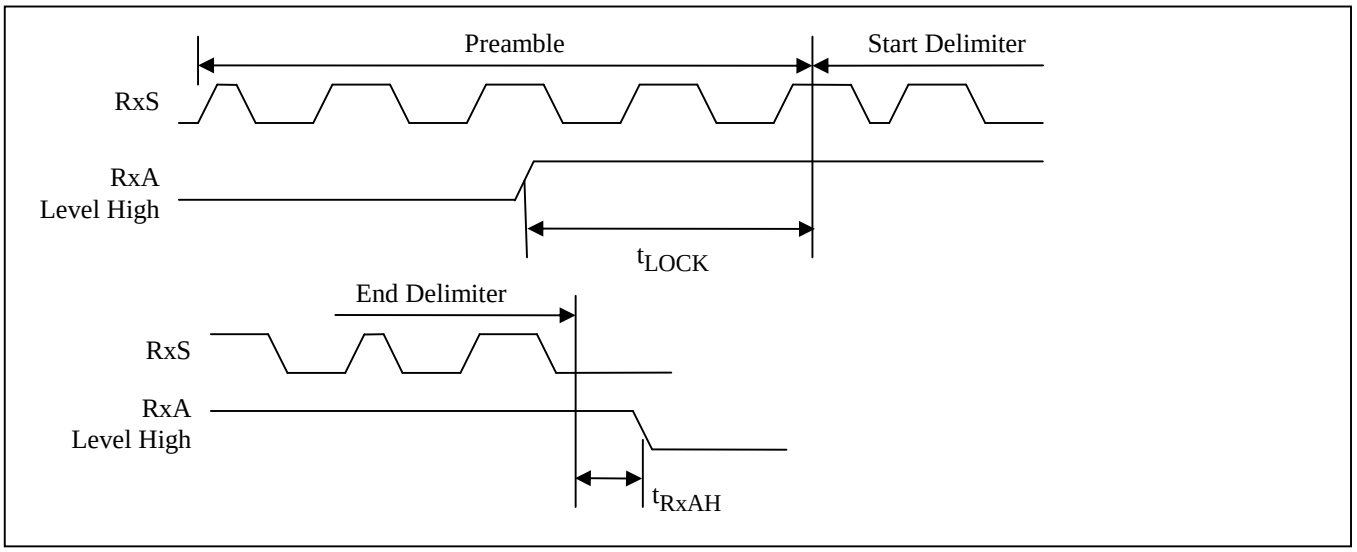

Figure 18: MAU Interface Receiver Timings

4.6 Other Timings

4.6.1 Reset Timings

Table 12: Reset Timings

Num	Description	Min	Max	Notes
t_{RST}	Reset active duration after the active clock	$3*T_{CLK}$		1
t_{RDLY}	Delay from inactive reset input to active chip select	$4*T_{CLK}$		

Notes:

1. RESETn input has to stay active while the power supply voltage is below minimum value.

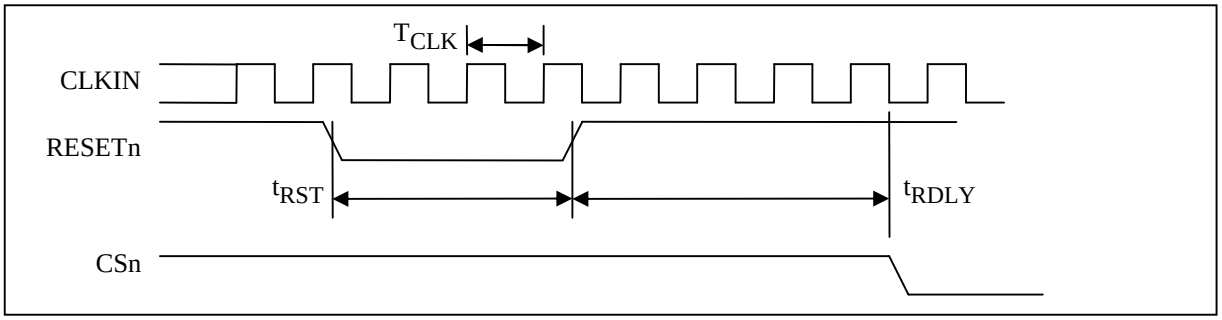

Figure 19: Reset Signal Timings

4.6.2 Interrupt Timings

Table 13: Interrupt Timings

Num	Description	Min	Max	Notes
t_{TXINTD}	Active INTn output to end of transmission delay	7 µs	10 µs	1
$t_{RXINTD1}$	End delimiter in RxS to active INTn output delay	6 µs	14 µs	2
$t_{RXINTD2}$	RQ end to active INTn output delay	1 µs	6 µs	3

Notes:

1. INTn becomes active before TxEn becomes inactive. The CPU can try to start the next transmission before TxEn for the current transmission becomes inactive and the next transmission is queued properly.
2. If end delimiter is not detected and RxA becomes inactive, then this delay is from the end of activity. If DMA is enabled, then the interrupt becomes active only after the receive FIFO becomes empty. The last received byte is available for transfer at the start of end delimiter. Therefore, in DMA mode, the FIFO is likely to become empty before the end delimiter is detected.
3. If DMA is enabled and the receive FIFO does not become empty until after the end delimiter is detected, then INTn becomes active this delay after last RQ.

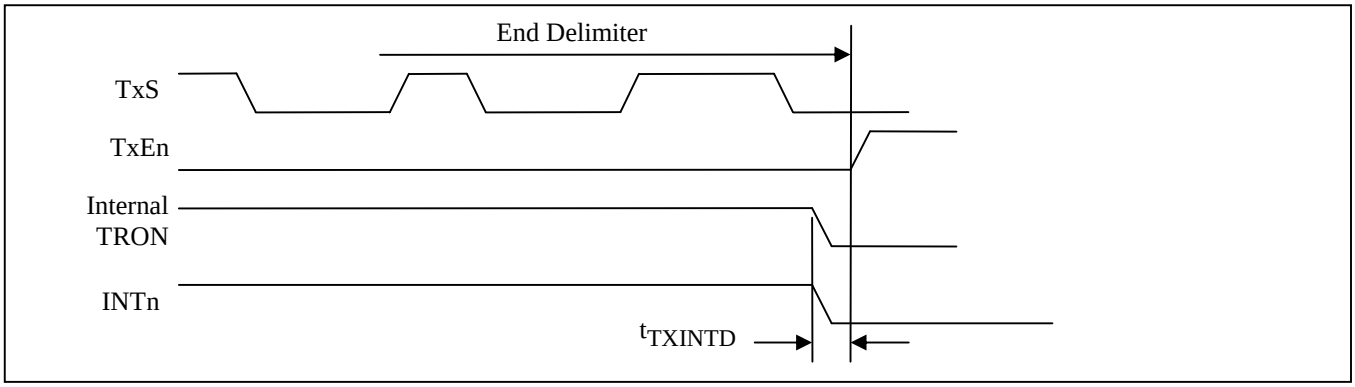

Figure 20: TED Interrupt Timings

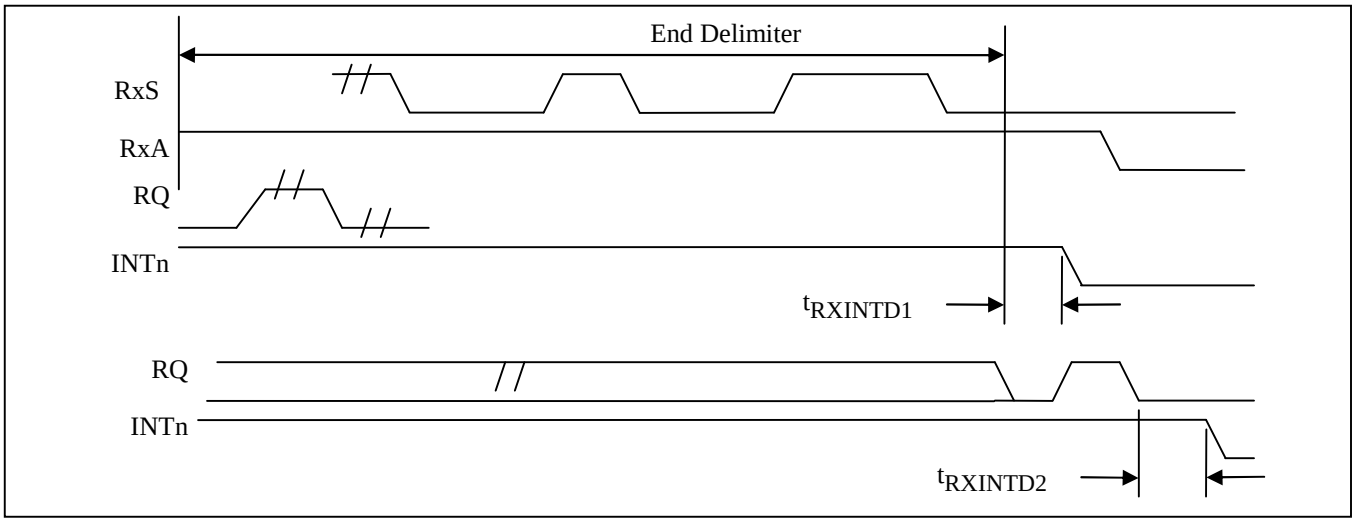

Figure 21: RED Interrupt Timings

5 PACKAGE

UFC100-L2 is available in 44 pin RoHS certified LQFP package. The dimensions are shown in Figure 22.

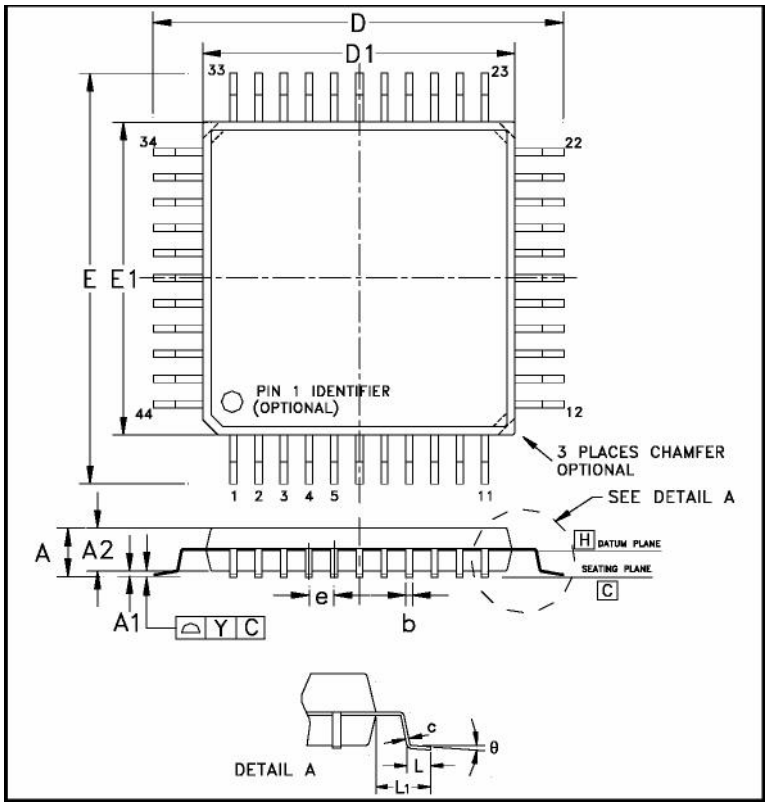

Figure 22: LQFP package dimensions

Table 14: LQFP package dimensions

Symbol	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.22	0.30	0.38	0.009	0.012	0.015
c	0.09		0.20	0.004		0.008
D	12.00 BSC.			0.472 BSC.		
E	12.00 BSC.			0.472 BSC.		
e	0.80 BSC.			0.031 BSC.		
D1	10.00 BSC			0.393 BSC.		
E1	10.00 BSC			0.393 BSC.		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
Y	0.10			0.004		
θ	0^o		7^o	0^o		7^o

Symbol	Parameter	Value	Units
Rth j-a	Thermal resistance from junction to ambient with no airflow	39.4	^{0} C/W
MSL	Moisture sensitivity level	3	
Reflow temperature	Maximum reflow soldering temperature	260	^{0} C